CLAIMS

What is claimed is:

1. A method for fabricating a memory device, the method comprising the steps of:

(a) providing a portion of a dual gate oxide in a periphery area of the memory device;

(b) simultaneously providing a dual gate oxide in a core area of the memory device and completing the dual gate oxide in the periphery area; and

(c) providing a nitridation process in both the core area and periphery area of the memory device subsequent to steps (a) and (b).

2. The method of claim 1 further comprising:

(d) depositing a layer of type-1 polysilicon in both the core area and periphery area of the memory device;

(e) depositing a layer of oxide nitride oxide over the layer of type-1 polysilicon; and

(f) removing the layer of oxide nitride oxide and a portion of the layer of type-1 polysilicon from the periphery area of the memory device.

3. The method of claim 2 wherein step (f) further includes removing approximately half the layer of type-1 polysilicon from the periphery area of the memory device.

4. The method of claim 3 further comprising:

(g) depositing a layer of type-2 polysilicon in both the core and periphery areas of the memory area.

5. A flash memory device, comprising;

a core area having a plurality of memory transistors comprising an oxide layer, a first poly layer, an interpoly dielectric layer, and a second poly layer; and

a periphery area having a plurality of transistors comprising an oxide layer, a portion of the first poly layer, and the second poly layer.

6. The flash memory device of claim 5 wherein the interpoly dielectric layer comprises oxide nitride oxide.

7. The flash memory device of claim 6 wherein the portion of the first poly layer in the periphery area comprises one half the first poly layer in the core area.

8. The flash memory device of claim 7 wherein the first poly layer comprises a type-1 polysilicon.

9. The flash memory device of claim 8 wherein the second poly layer comprises a type-2 polysilicon.

10. A method for fabricating a memory device, the method comprising the steps

of:

(a) providing a portion of a dual gate oxide in a periphery area of the memory device;

(b) simultaneously providing a dual gate oxide in a core area of the memory device and completing the dual gate oxide in the periphery area;

(c) providing a nitridation process in both the core area and periphery area of the memory device subsequent to steps (a) and (b);

(d) depositing a layer of type-1 polysilicon in both the core area and periphery area of the memory device;

(e) depositing a layer of oxide nitride oxide over the layer of type-1 polysilicon; and

(f) removing the layer of oxide nitride oxide and a portion of the layer of type-1 polysilicon from the periphery area of the memory device.

11. The method of claim 10 wherein step (f) further includes removing approximately half the layer of type-1 polysilicon from the periphery area of the memory device.

12. The method of claim 11 further comprising:

(g) depositing a layer of type-2 polysilicon in both the core and periphery areas of the memory area.